In the Claims

CLAIMS:

Claims 1-8 have been cancelled.

9. (Original) A method of receiving information using a direct sequence code division multi-access receiver, the method comprising the steps of:

receiving a first signal that includes one or more direct sequence codes;

sampling the signal to obtain a series of complex chip values;

multiplying each Nth complex chip value in the series, by the complex conjugate of another complex chip value in the series that is separated from the Nth complex chip value by a predetermined number of places to obtain a differentially decoded series;

performing a vector dot product between a plurality of bit length sub-series selected from the differentially decoded series, and a reference vector to obtain a series of dot product values; and

comparing each of the series of dot product values to one or more predetermined constants.

B1 cont

10. (Original) The method according to claim 9 wherein the step of multiplying comprises the sub-step of:

multiplying each Nth complex chip value in the series, by the complex conjugate of a another complex chip value in the series that is adjacent to the Nth complex chip value to obtain the differentially decoded series.

11. (Original) The method according to claim 9 wherein the step of receiving a first signal comprises the sub-step of:

receiving a signal consisting of multiple copies of a single direct sequence code interspersed with null periods.

12. (Original) The method according to claim 11 wherein the step of performing a dot product includes the sub-step of:

performing a vector dot product between a plurality of bit length sub-series selected from the differentially decoded series, and a reference vector that is equal to a vector obtained by multiplying each Nth element in the single direct sequence code, by

another element in the single direct sequence code that is separated from the Nth element by the predetermined of places number, to obtain a series of dot product values.

13. (Original) The method according to claim 12 wherein the step of comparing each of the series of dot product values to one or more predetermined constants includes the sub-step of:

comparing each of the series of dot product values to a first constant.

14. (Original) The method according to claim 9 wherein the step of receiving a first signal that includes one or more direct sequence codes comprises the sub-step of:

receiving a signal that includes a first direct sequence code and a second direct sequence code.

15. (Original) The method according to claim 14 wherein the step of performing a dot product includes the sub-step of:

B1 Cont

performing a vector dot product between a plurality of bit length sub-series selected from the differentially decoded series, and a reference vector that is substantially equivalent to a vector obtained by subtracting a first component vector that is obtained multiplying each Nth element in the first direct sequence code, by another element in the first direct sequence code that is separated from the Nth element in the first direct sequence code by the predetermined number from a second component vector that is obtained multiplying each Nth element in the second direct sequence code, by another element in the second direct sequence code that is separated from the Nth element in the second direct sequence code by the predetermined number, to obtain a series of dot product values.

16. (Original) The method according to claim 15 wherein the step of comparing each of the series of dot product values to one or more predetermined constants includes the sub-step of:

comparing each of the series of dot product values to a constant that is about zero.

17. (Original) The method according to claim 9 wherein the step of receiving a first signal that includes one or more direct sequence codes comprises the sub-step of:

receiving a signal that includes 2^N distinct direct sequence codes, where N is an integer.

18. (Original) The method according to claim 17 further comprising the step of:

obtaining the reference vector that is equal to a vector obtained by:

processing each distinct direct sequence code by multiplying each Nth element in the distinct direct sequence code, by another element in the distinct direct sequence code that is separated from the Nth element by the predetermined number, to obtain 2^N distinct differentially decoded vectors;

multiplying each distinct differentially decoded vector by a distinct constant to obtain a plurality of component vectors; and

summing the component vectors.

19. (Original) The method according to claim 18 wherein the step of comparing each of the series of dot product values to one or more predetermined constants comprises the sub step of:

comparing each of the series of dot product values to a plurality of distinct constants.

B1 cont

20. (Original) The method according to claim 9 wherein the step of receiving the first signal that includes one or more direct sequence codes comprises a sub-step of:

in-phase and quadrature demodulating a received RF signal to obtain a complex demodulator output signal;

low pass filtering the complex demodulator output signal to obtain the first signal.

21. (Original) The method according to claim 20 wherein the step of low pass filtering comprises the sub-step of:

filtering the demodulator output with a chip pulse match filter.

22. (Original) The method according to claim 9 wherein the step of receiving a first signal comprises the sub-step of:

receiving a signal that includes a direct sequence code having at least about seven elements

23 (Original) The method according to claim 9 wherein the step of receiving a first signal comprises the sub-step of:

receiving a signal that includes a direct sequence code having at least about 15 elements.

Claims 24-28 have been cancelled

29. (Original) A direct sequence code division multi-access information receiver comprising:

a channel interface for receiving a signal including a sequence of complex chip values;

a multiplier for multiplying each Nth chip value in the sequence of chip values by the complex conjugate of another chip value in the sequence of chip values that is separated from the Nth by a predetermined number of places to obtain one or more chip-by-chip differentially decoded sequences;

a dot product performer for performing a dot product between the one or more chip-by-chip differentially decoded sequences and a one or more reference vectors and outputting one or more dot product values; and

a discriminator for identifying one or more information conveying symbols based on the one or more dot product values.

B1 cont

30. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the channel interface comprises:

an antenna for receiving an RF signal;

a I/Q demodulator coupled to the antenna for receiving the RF signal and outputting a complex demodulated signal;

a low pass filter coupled to the demodulator for receiving the complex demodulated signal, and outputting a complex baseband signal; and

an analog-to-digital converter coupled to the low pass filter for sampling the complex baseband signal to obtain the sequence of complex chip values.

31. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the multiplier comprises: .

a processor programmed to:

multiply each Nth complex chip value in the sequence of complex chip values by the complex conjugate of another complex chip value in the sequence of chip values that is separated from the Nth by a predetermined number of places.

32. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the dot product performer comprises:

a processor programmed to:

compute one or more dot products between the one or more chip-by-chip differentially decoded sequences and a one or more reference vectors and outputting one or more dot product values.

33. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the discriminator comprises:

a comparator for comparing the one or more dot product values to one or more constants that are associated with the one or more information carrying symbols.

34. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the dot product performer comprises:

a dot product performer for performing a dot product between the one or more chip-by-chip differentially decoded sequences and a reference vector that includes a first pseudo noise sequence that is associated with a first information symbol , vectorially added to a second pseudo noise sequence that is associated with a second information symbol and outputting one or more dot product values.

B1 cont

35. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein:

the dot product performer comprise a dot product performer for performing a dot product between the one or more chip-by-chip differentially decoded sequences and a single reference vector and outputting one or more dot product values; and

the discriminator comprises a comparator for comparing each of the one or more dot product values to a threshold value, and outputting a first bit value in the case that a dot product value exceeds the threshold.

36. (Original) The direct sequence code division multi-access information receiver according to claim 29 wherein the multiplier comprises:

a multiplier for multiplying each chip value in the sequence of chip values by the complex conjugate of an adjacent chip value in the sequence of chip values to obtain one or more chip-by-chip differentially decoded sequences.

Claims 37-43 have been cancelled.

44. (Original) A computer readable medium having programming instruction for operating a direct sequence code division multi-access receiver, including programming instructions for:

reading a series of complex chip values;

multiplying each Nth complex chip value in the series, by the complex conjugate of another complex chip value in the series that is separated from Nth complex chip value by a predetermined number of places to obtain a differentially decoded series;

performing a vector dot product between a plurality of bit length sub-series selected from the differentially decoded series, and a reference vector to obtain a series of dot product values; and

comparing each of the series of dot product values to one or more predetermined constants.

B1 Cont'd